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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Timothy M. Lacey et al.
Serial No.:	09/475,879
Title:	PROGRAMMABLE LOGIC DEVICE
Filed:	December 30, 1999
Examiner:	Tran, A.
Art Unit:	2819

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TECHNOLOGY CENTER 2800

DECLARATION OF DAVID L. JOHNSON UNDER 37 C.F.R. 1.131

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

I, David L. Johnson hereby declare and state:

1. I was employed by Cypress Semiconductor Corporation from 10/1994 to 3/2000, where my job title was DEPARTMENT MANAGER.

2. Prior to March 24, 1999, Timothy M. Lacey and I conceived the invention claimed in the above-identified patent application as shown by the pages of the Ultra39000 Family Architecture Spec attached as Exhibit A. The redacted dates on the Document History Page (i.e., page 98 of 98) show document issue dates which were before March 24, 1999 (see MPEP §715.07, "ESTABLISHMENT OF DATES", allowing allegation that acts referred to occurred prior to a specified date where the actual dates have been redacted).

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3. The invention claimed in the above identified application was diligently reduced to practice as shown by the attached Exhibits B and C. Exhibit B is a copy of a Cypress Semiconductor Invention Disclosure Form for the present invention. The notations in the lower right hand corner of pages 1 through 6 of 6 in Exhibit B show a date of July 14, 1999. Dates pertaining to the conception of the present invention which have been redacted occurred prior to March 24, 1999 (see MPEP §715.07, "ESTABLISHMENT OF DATES", allowing allegation that acts referred to occurred prior to a specified date where the actual dates have been redacted). Exhibit C is a copy of a letter dated September 13, 1999 from Cypress Semiconductor's Corporate Counsel engaging Applicants' representative's law firm to prepare the application filed December 30, 1999.

4. In my opinion, the attached Exhibits A and B corresponding to the Ultra39000 Family Architecture Spec and the Cypress Semiconductor Invention Disclosure Form, respectively, describe the claimed invention and convey information sufficient to enable one skilled in the relevant art to make and use the claimed invention.

5. To the best of my knowledge, no working samples of the Delta 39K family were sent to any party outside Cypress until December 30, 1999 or later.

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6. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

David L. Johnson

12/21/2001
Date

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CYPRESS SEMICONDUCTOR EXHIBIT A

Ultra39000 Family Architecture Spec

Table of Contents

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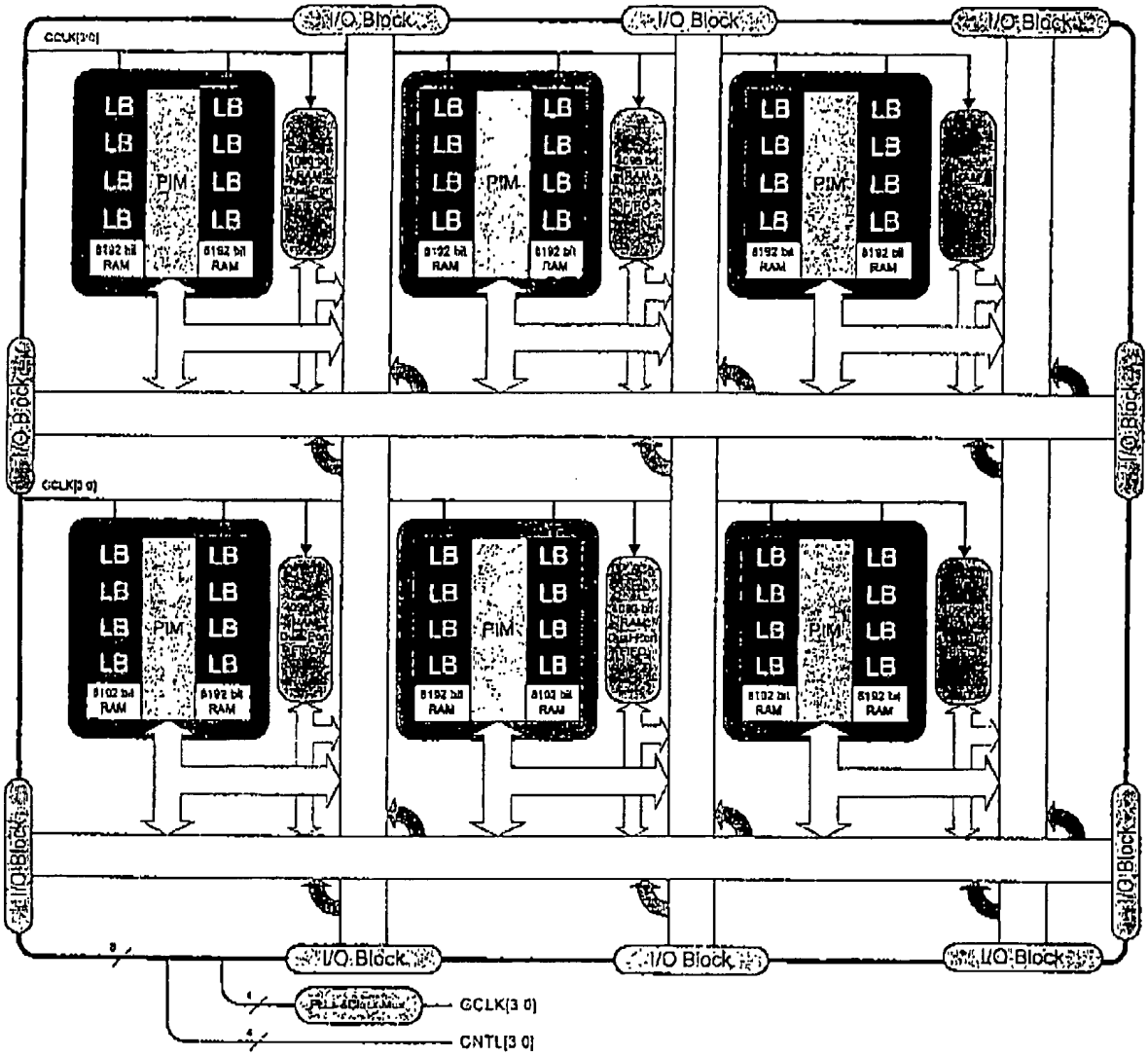

Figure 8.1: Block diagram of CY39K768

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CYPRESS SEMICONDUCTOR

Document History Page

Document Title: Ultra39000 Family Architecture Specification
Document Number: 40-00129

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	59138	[redacted]	MMQ	Original document
*A	60891	[redacted]	TLM	Correct errors and incorporate architecture changes

Distribution: E-OREGON, E-CTI

Posting: None

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EXHIBIT B

Cypress Semiconductor Invention Disclosure Form

1. INVENTOR

A. Name: Timothy M. Lacey Empl. No: [redacted] Ext. No: [redacted]
Citizenship: USA Dept No: NEDC Home No: [redacted]
Home mailing address: [redacted]

B. Name: David L. Johnson Empl No: [redacted] Ext. No: [redacted]
Citizenship: USA Dept No: PLD Home No: [redacted]
Home mailing address: [redacted]

C. Name: Jeffery Mark Marshall Empl No: [redacted] Ext. No: [redacted]
Citizenship: USA Dept No: PLD Home No: [redacted]
Home mailing address: [redacted]

2. TITLE OF INVENTION:

Improved programmable logic device architecture

3. CONCEPTION OF INVENTION

A. Date of first drawings: [redacted]
Where can first drawings be found: Ultra39000 Family Architecture Spec

B. Date of first written description: [redacted]
Where is the description: Cypress Memolog:
BXM#2 SRAM CPLD MKT[redacted]
TL#165[redacted] ALG#213[redacted]
BWG#68[redacted], MMQ#[redacted]

C. Date of first oral disclosure to others: [redacted]
To whom: Chris Norris

4. CONSTRUCTION OF DEVICE

A. Date completed: October 99 (forecast)
B. Was a prototype made: No
C. By whom made: Cypress Semiconductor
D. Where can the prototype be found: N/A

5. TEST OF THE DEVICE

A. Date tested: February 00 (forecast)
B. Witness(es): N/A
C. Results: N/A

6. SALE

A. Was invention sold?: No
B. Date of first sale: N/A

Inventor:_____ Date:_____
Inventor:_____ Date:_____
Inventor:_____ Date:_____
Witness. Read, and Understood by:_____ Date:_____
Witness. Read, and Understood by:_____ Date:_____

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Cypress Semiconductor Invention Disclosure Form

7. USE

   A. Is invention presently being used: Yes
   B. Are there specific plans for its use in the near future?: Yes, the Delta39K family of PLD products.

8. RELATED PRINTED PUBLICATIONS, PATENTS, PATENT APPLICATIONS:

   List of 39K disclosures:

   Search of Altera and Xilinx patents.

9. DURING PERFORMANCE OF GOVERNMENT CONTRACT WAS INVENTION

   A. Conceived: No
   B. Constructed: No
   C. Tested: No
   D. Contract No: N/A

1. **General purpose of invention. State in general terms the objects of the invention.**

The purpose of the invention is to provide a programmable logic architecture that has all the benefits of traditional CPLD and FPGA architectures with out the disadvantages.

2. **Describe old method(s), if any, of performing the function of the invention.**

Traditionally there are two types of programmable logic architectures: CPLD's and FPGA's.

An example of a CPLD architecture is Cypress' 37000. The architecture is constructed as a one-dimensional array of logic blocks made of 16 macrocells and a product term array connected through a single central interconnect scheme. It achieves high performance by being able to complete a complex logic function in a single pass of the logic array, and has predictable timing by having every output or I/O pin connected to every logic block input through a central interconnect structure. The product is non-volatile by using a EEPROM process.

An example of an FPGA architecture is Xilinx 4000. This architecture is constructed from a two dimensional array of logic blocks called CLB's that are made from 4 input look-up-tables (LUTs) and flip-flops; the LUTs can be used as distributed memory blocks. The architecture supports a low standby power and the most advanced technology available because the LUT's use a simple logic CMOS process. It also achieves high density because the 2 dimensional array of CLB's and the segmented interconnect structure scale very well.

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3. **Indicate the disadvantages of the old method(s).**

CPLD architectures have the following disadvantages:

- Complex process technology hurts performance and cost.
- High standby power limits capacity and applications.
- No available on chip RAM
- Maximum capacity of the device is limited by interconnect structure performance, power, technology and die cost.
- Core voltages, I/O voltages, and I/O standards are not flexible.
- I/O cell with synchronous OE to support NoBL or ZBT.

FPGA architectures have the following disadvantages:

- Volatile process requires a FLASH/EEPROM to be added to the design.
- Segmented routing architecture limits performance, and makes timing unpredictable.
- Dual port or FIFO memory is slow and inefficient to implement with LUTs.
- Complex design in process because products do not have predictable timing, short compile times, in-system-reprogrammability (ISR), and pin fixing.
- Core voltage is not flexible, and is driven by the current process. Product migration is made very difficult.
- No support for JTAG boundary scan.

4. **Describe the construction of your invention, showing the changes, additions and improvements over the old method.**

The construction of the invention is described in detail in the attached Ultra39000 Family Architecture Spec. The 39K architecture is an extension to Cypress' Ultra37000 architecture. The Delta39000 CPLD family contains several basic architectural components that are assembled in differing numbers of rows and columns. The main architectural components include logic block clusters, channel memory, cluster memory, horizontal routing channels, vertical routing channels, I/O blocks, and the control block.

Instead of using an EEPROM technology the 39K is using an advanced CMOS logic process. The product will still be capable of being non-volatile by having a separate non-volatile storage device within the same package. This will put the product technology two generations ahead of all other CPLD's. The product will support external core voltages of 3.3V, 2.5V, or 1.8V through the use of an internal voltage regulator. This allows the customer to choose the most painless core voltage, and migrate to the latest technology with out changing the power supply scheme.

Instead of using a single global interconnect scheme the 39K is using a hierarchical two-dimensional routing scheme. The logic blocks are grouped in clusters. These clusters

Inventor:_____ Date:_____
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are placed in a two dimensional array that uses horizontal routing channels to connect in the x axis, and vertical routing channels to connect in the y axis.

Two blocks of highly configurable RAM are placed inside each of the clusters. This RAM can be configured as asynchronous, synchronous inputs, synchronous outputs, pipelined, x1, x2, x4, x8, look up tables, and ROM code. The RAM is placed inside of the cluster to achieve high performance with the local logic blocks.

Next to each cluster is a configurable channel memory that it connected to the vertical and horizontal routing channel. The channel memory is configurable as a synch dual port, asynchronous dual port, synchronous FIFO, x1, x2, x4, and x8. This memory is placed in the routing channels to achieve high performance with the I/O blocks.

Unlike the 37K the I/O cells are not connected to the logic block macrocells. Instead the 39K has an I/O block that contains 21 I/O cells that is connected to the end of each horizontal or vertical routing channel. The I/O cell also contains an input or output register, oe register, programmable slew rate control, and programmable bus hold. The 39K has four global inputs that can be used for output enables, register resets, and register clock enables. The separate I/O block allows for improved design "fitting", pinout flexibility, and I/O performance. The I/O blocks are combined to form I/O banks that allow the I/O to support all of the current I/O standards within the 1.5V to 3.3V range.

Like the 37K the 39K supports JTAG boundary scan, and the JTAG programming standard STAPL. The 39K also supports JTAG INTEST, and full scan. The 39K support several configuration mode that use compression/de-compression to reduce the storage requirement, and error checking to detect problems. These configuration modes include master serial, master parallel, and JTAG (IEEE std 1149.1 interface).

The 39K contains four global clocks that go to every register. The part also has a PLL that can deliver to any or all of the four clocks a multiplied, divided, phase shifted, or de-skewed version of the clock 1 input.

To reduce the power of the device no sense amps are used on the part. The logic block AND plane and OR plane use a complex CMOS logic gate instead of the traditional high power sense amps. The rams use a novel ATD circuit to remove the need for RAM sense amps, and to prevent DC power consumption.

5. Give details of the operation if not already described under 4.

Attached to this disclosure is the Ultra39000 Family Architecture Spec, which describes the architecture in detail.

6. State the advantages of your invention over what has been done before.

Advantages over what has been done before:

- Removed need for EEPROM and high voltage to get advanced process technology, which improves performance and cost.
- Non-volatile part uses separate off chip non-volatile storage device within the same package.

Inventor:_____ Date:_____
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- Removed DC power consumption by using complex CMOS gates for the AND and OR plane instead of sense amps.
- Added large configurable single port RAM, dual port RAM, and FIFO's.
- Using novel ATD scheme to remove RAM DC power.
- Largest CPLD device on the market because of advanced process, hierarchical (multi-stage PIM) routing structure, reduction of power.
- I/O cells are configurable to support I/O standards LVCMOS, LVTTL, HSTL, SSTL, PCI, and GTL+; I/O cells are banked to support multiple standards within the same product.
- Programming of device is achieved in-system using the STAPL programming interface.
- The hierarchical PIM based routing structure allows for a high-speed compact routing structure that allows for a simple timing model.
- Including dedicated dual port memory logic and arbitration, and FIFO memory logic and flags improve memory performance and increases the capacity of the device.
- The global nature of the routing structure means that no place and route step is needed. This reduces compile time, and increases predictability. The routing structure insures pin out flexibility. And the STAPL interface allows the part to be reconfigured in-system.
- The on-chip voltage regulator allows for a flexible core voltage.
- JTAG boundary scan (including INTEST) allows for easy board, and design debug.

7. Indicate any alternate method of construction.

The size and number of the logic blocks, clusters, single port RAM, dual port RAM, FIFO RAM, I/O blocks, PLLs, and routing channels could be smaller or larger. The architecture could be extended to more levels of hierarchy; for example, there could be groups of clusters called pods that could be connected with a another level of vertical and horizontal routing. The architecture could be constructed without some of the base components like the PLL, Regulator, channel memory, or the cluster memory.

8. If a joint invention, indicate what contribution was made by each inventor.

The architecture definition was a large collaborative effort that extents far beyond the three inventors presented in this disclosure.

9. Features which are believed to be new.

First PLD to:

- Use a separate off chip non-volatile storage device within the same package.

Inventor:_____ Date:_____
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Inventor:_____ Date:_____
Witness, Read, and Understood by:_____ Date:_____
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- Including dedicated dual port memory logic and arbitration, and FIFO memory logic and flags improve memory performance and increases the capacity of the device.
- Have two types of memory, at different levels of the hierarchy. Single port RAM tightly coupled to logic blocks, and the Dual port RAM tightly coupled to the I/O cells, and the global routing.
- Use a novel ATD scheme to remove RAM DC power.
- Have a hierarchical PIM based routing structure providing a high-speed compact routing structure that allows for a simple timing model.
- Have an on-chip voltage regulator that allows for a flexible core voltage.
- Have JTAG scan modes including INTEST to allow for easy system, and design debug.

First CPLD to:

- Remove the need for EEPROM and high voltage to get advanced process technology, which improves performance and cost.
- Remove DC power consumption by using complex CMOS gates for the AND and OR plane instead of sense amps.
- Have large configurable single port RAM, dual port RAM, and FIFO's with dedicated logic and features to improve performance.
- Have I/O cells that are configurable to support multiple I/O standards LVCMOS, LVTTL, HSTL, SSTL, PCI, and GTL+; I/O cells that are banked to support multiple standards within the same product.

10. State opinion of relative value of invention.

The future of Cypress's PLD business depends on the success of the 39K family, and our ability to protect ourselves from litigation.

Inventor:_____ Date:_____
Inventor:_____ Date:_____
Inventor:_____ Date:_____
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EXHIBIT C

CYPRESS

September 13, 1999

Andrew D. Fortney, Ph.D., Esq.
CYPRESS SEMICONDUCTOR CORP.
3939 N. First Street
San Jose, CA 95134

Mr. Christopher Maiorana
CHRISTOPHER P. MAIORANA, P.C.
21643 E. Nine Mile Road, Suite A
St. Clair Shores, Michigan 48080

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RE: New U.S. Patent Applications
Our Refs: CD99047 and CD99067

Dear Chris:

Please find enclosed an invention disclosure by Cypress employees Timothy M. Lacey, David L. Johnson and Jeffery Mark Marshall entitled IMPROVED PROGRAMMABLE LOGIC DEVICE. (I would like to delete the word "Improved" from the title.) The invention was presented at a patent review meeting at Cypress. The consensus was that at least two ideas therein are patentable. We would appreciate your preparation of two full applications to file with the Patent and Trademark Office, one directed to the overall architecture, and one directed to the "channel memory" aspect.

Please contact Tim (phone: [redacted]) to clarify points in the accompanying paperwork and discuss strategies for drafting the applications. Please copy me all correspondence sent to the inventors. We would also like you to review the invention disclosure for additional patentable subject matter. Copies of other patent applications filed on various aspects of this project (the "Delta 39K" PLD) are being sent separately. Please review the pending applications and provide me with a list of those subject matter topics in the enclosed invention disclosure for which we could pursue patent protection.

Please note that we have set a budget of [redacted] for the preparation of each application and [redacted] for the list of other patent topics. Please contact me if you think you may exceed the budget. Our goals are to receive a first draft within about 6 weeks and to file each application within 13 weeks. Thank you for your cooperation with our efforts.

Sincerely,

Andrew D. Fortney, Ph.D., Esq.
Senior Corporate Counsel/Director of Intellectual Property

Enclosures: Invention Disclosure; references
cc (letter only): Paul Keswick, Tim Lacey, David Johnson, Mark Marshall, Jack Berg

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